An 8-bit 1.8 V 500 MS/s CMOS DAC with a Novel Four-Stage Current Steering Architecture

Santanu Sarkar*, Ravi sankar Prasad†, Sanjoy Kumar Dey‡, Vinay Belde* and Swapna Banerjee*
*Department of Electronics and Electrical Engineering
Indian Institute of Technology, Kharagpur 721302
Email: ss.saan@gmail.com, rsprasad@ti.com, sankudey@rediffmail.com,
vinaybelde@gmail.com, swapna@ece.iitkgp.ernet.in
†Texas Instruments, Bangalore, India
‡Freescale Semiconductor India Private Ltd., Noida, India

Abstract—This paper presents an 8 bit 1.8 V 500 MSPS digital-to-analog converter using 0.18 μm double poly five metal CMOS technology for frequency domain applications. The proposed DAC is composed of four unit cell matrix. A novel decoding logic is used to remove the Inter Block Code Transition (IBT) glitch. The proposed DAC shows less number of switching for a monotonic input and the product of number of switching and the current value associated with switching is also less than the segmented DAC. The SPICE simulated DNL and INL is 0.1373 LSB and 0.331 LSB respectively and are better than the segmented DAC. The proposed DAC also shows better SNDR and THD than the segmented DAC. The MATLAB simulated THD, SFDR and SNDR is more than 45 dB, 35 dB and 44 dB respectively at 500MS/s with a 10 MHz input sine wave with incoherent timing response between current switches.

I. INTRODUCTION

For high speed and high resolution DACs, current steering architectures are preferably used due to its capability of driving resistive loads without buffering [1]. Thermometer architecture of current steering DACs is inherently monotonic, shows good linearity and absence of glitch. The requirement of matching of the current sources is also relaxed up to 50% [2]. Unary DAC suffers from design complexity, large area and large power dissipation. On the other hand, binary architecture is simple and require less area and less power, as no decoding logic is required. But the major drawback of binary architecture is the degraded performance due to glitch, mainly at midcode transitions and tough matching requirement of the current sources [3]. So a trade off between thermometer and binary architecture is made in segmented architecture. In segmented architecture the DAC is divided into two sub-DACs, where MSB block is implemented in thermometric fashion for better accuracy and LSB block use the binary scheme. For 8 bit resolution the optimum segmentation is calculated as 6+2 by Lin and Bult [2]. The segmented architecture reduces the complexity of the decoding logic and hence area is substantially reduced compared to unary DAC. But the problems of the segmented architecture is the rapid degradation of dynamic performance at higher frequency, delay mismatch between MSB and LSB block and Inter block code Transition (IBT) glitch. For a rising monotonic input every change in the MSB bit requires switching OFF all the current sources in the LSB block and turning ON one current source in the MSB block. Lack of synchronisation in the timing of the control signals of the two block results into severe glitch, termed as IBT glitch. IBT glitch can become a major source of non-linearity introducing noise and thereby degrading the overall dynamic performance.

This paper proposes a novel architecture which eliminates the IBT glitch and shows better Signal-to-Noise Ratio compared to segmented DAC. The proposed architecture is simple and needs less number of decoder compared to unary DAC. Mid-code glitch and most of the major carry glitch is eliminated and the matching requirement is also relaxed compared to binary DAC. Improved glitch energy performance and improved SNDR and SNR make this DAC a highly suitable candidate for digital communication and video applications, where glitch noise performance and SNDR plays a very significant role.

II. ARCHITECTURAL CHOICES AND CIRCUIT DESIGN

A. Block Diagram

The block diagram of the proposed DAC architecture is shown in Fig. 1. The block consists of input data registers, clock buffers, one row and column decoder and four unit current cell matrix named as "A", "B", "C" and "D". The digital inputs are first clocked into input registers. Then the first three MSBs are column decoded, the next two bits are row decoded, and the final three LSB bits D2, D1 and D0 are sent to the local decoding logic for the current cell matrix of "D";C" and "B" respectively. There are 31 cells in the "A" matrix and each of the "B", "C" and "D" matrix contains 32 cells. The darkened cell at the corner of the "A" matrix is not used. The current source value in the "A" and "B" matrix is equal to \( I_{LSB} \) current, and the current source value of the "C" and "D" matrix are \( 2I_{LSB} \) and \( 4I_{LSB} \) respectively.

B. Operation Principle

In this proposed architecture the complete N bit DAC is divided into numbers of M-bit sub-DACs and 1-bit sub-DACs. Each of these sub-DACs is basically a binary DAC. For this case, M is equal to 3 and N is equal to 8. Selection of these 1-bit and 3-bit sub-DACs is done by same row and column...
decoder as shown in Fig. 1. The global row and column decoders work in thermometric manner and within each selected 3-bit binary sub-DAC current sources are switched in binary fashion, locally. Operation principle of the proposed encoding scheme is illustrated with an example of 4 bit DAC in Fig. 2. The 4-bit DAC consists of one 1-bit sub-DAC and two 3-bit sub-DAC. The bordered blocks represent selected sub-DAC and the darkened current cell implies it is switched ON. Fig. 2 shows that when the input code value is one the current source of the second 3-bit sub-DAC is turned on. The LSB is switched OFF. In similar manner for input of seven all the three current sources of the first 3-bit sub-DAC is turned ON. When the input is eight, this three current cells of the first sub-DAC, remains ON and another one current source of the 1-bit sub-DAC is turned ON making a total current of \( 8I_{LSB} \) as required. This operation is unlike usual binary DAC where it is required to turn ON a current source of \( 8I_{LSB} \) and simultaneously switching OFF the three cells. Keeping this three cells ON and turning ON only one extra cell removes the IBT glitch associated with transition from 0111 to 1000. For input bit of nine all the current sources of first 3-bit sub-DAC and 1-bit sub-DAC remain ON and the \( I_{LSB} \) source of the second 3-bit sub-DAC is turned on. The speciality of this encoding scheme is that, for an increasing monotonic input the sub-DAC once fully turned ON, remains ON. The operation proceeds in similar manner till last code.

For N-bit, the proposed DAC, realized with M-bit sub-DACs has \( 2^{N-M} - 1 \) number of 1-bit Sub-DAC, and \( 2^{N-M} \) number of M-bit sub-DAC. In order to get the maximum benefit of the proposed scheme, the number M of the sub-DAC can be chosen as 2, whose only major carry glitch occurs due to transition of bit D1 and D0 from 01 to 10, which is very insignificant in the overall system, but in that case the number of current cells will increase and we have to compromise with power. Since the glitch generated due to sub-DACs are small and distributed, they result in a smaller higher frequency harmonics lying outside the bandwidth of interest, unlike segmented scheme having larger glitches concentrated at the LSB causing harmonics in the output spectrum inside the bandwidth of interest. As a result we get better SNR and SNDR compare to segmented counter part.

### C. Unit Current Cell

Fig. 3 shows the circuit of one unit current cell of ”A” matrix. It consists of an analog part and a digital part. The analog part consists of a differential switch and a cascoded current source. Cascoded source is used to increase the output impedance. The analog part consists of a decoding logic and a latch. The decoding logic of the ”A” matrix is equivalent to an AND-OR gate function [4]. The decoding logic for the ”B”, ”C” and ”D” is equivalent to an AND-AND-OR gate function as shown in Fig. 4. The controlling LSB bit changes for different matrix, for ”B”, ”C” and ”D” block they are D0, D1 and D2 respectively. DeMorgan’s Law is used for the decoder implementation [5].

### III. COMPARISON OF SWITCHING PHENOMENON

At high speed, switching is a major concern in current steering architecture, the dynamic performance of the DAC largely depends on switching. Here for a monotonic input the switching phenomenon of the proposed DAC and other three
DACs are analyzed. For thermometer architecture one single cell is switched ON for an increase in the digital input code, so the total number of switching is equal to the total number of current sources. Hence for N bit resolution,

\[
S_{Unary} = 2^N - 1
\]

(1)

Therefore \( S_0 = 2^N - 1, S_1 = 2^{(N-1)} - 1, \ldots, S_{(N-1)} = 2^1 - 1. \)

On summing we get,

\[
S_{Binary} = \left\{2^N + 2^{(N-1)} + \ldots + 2^1\right\} - N
\]

(3)

In segmented DAC, the total number of switches turning ON/OFF comprises of switches switching. i) in MSB block i.e. each only once, ii) in LSB binary block which is repeated as many times MSB bit changes and iii) in LSB binary sub-DAC at Inter block code Transition, which is equal to the product of the number of current cells in the two sub-blocks. Considering m bits for LSB binary DAC, total number of switching for segmented DAC is calculated as below.

\[
S_{Seg} = \left\{2^{(N-m)} - 1\right\} + 2^{(N-m)} \times \left\{2^{(m+1)} - 2 - m\right\} + \left\{2^{(N-m)} - 1\right\} m
\]

(4)

In the proposed architecture we considered that N bit DAC is realized by M bit binary sub-DAC.Total number of switches turning ON/OFF, comprises of i) number of 1 bit sub-DAC and ii) switches switching in the M bit sub-DAC multiplied by the total number of M bit sub-DAC.

\[
S_{Proposed} = \left\{2^{(N-M)} - 1\right\} + 2^{(N-M)} \times \left\{2^{(M+1)} - 2 - M\right\}
\]

(5)

So, the total number of switching in the proposed DAC is less than the segmented DAC.

### IV. Switching and Signal Step Magnitude Product Comparison

Glitches show code dependency, thereby larger code value may generate higher non-linearities. To evaluate D/A converter for this effect, the product of the number of switching of the switches and the magnitude of the current value being switched are calculated for different architectures. This product is termed as Q here. For thermometer architecture

\[
Q_{Unary} = S_{Unary}I_{LSB} = (2^N - 1)I_{LSB} = 255I_{LSB}
\]

(6)

For Binary architecture, Q for current source at bit Di is termed as \( Q_i \), and can be easily calculated as shown below.

\[
Q_i = S_i 2^i I_{LSB}
\]

(7)

Hence summing the values for \( i=0 \) to \( i=N \), we get

\[
Q_{Binary} = \left\{N2^N - \left\{2^0 + 2^1 + 2^2 + \ldots + 2^{(N-1)}\right\}\right\} I_{LSB}
\]

(8)

\[
= 1793I_{LSB}
\]

For segmented architecture, as like the switching calculation, the product Q comprises of i) \( Q \) value for the MSB unary sub-DAC, ii) \( Q \) value for the LSB binary sub-DAC multiplied with \( 2^{(N-m)} \) and iii) total value of current in LSB binary sub-DAC multiplied with \( 2^{(N-m)} - 1 \).

\[
Q_{Seg} = \left\{2^{(N-m)} - 1\right\} 2^m + \left\{2^m(m-1) + 1\right\} \times \left\{2^{(N-m)} - 1\right\} 2^m I_{LSB}
\]

(9)

\[
= 761I_{LSB}
\]

For the proposed architecture, \( Q \) comprises of i) Number of 1 bit sub-DAC and ii) \( Q \) value of the M-bit sub-DAC multiplied with the total no of M-bit sub-DAC.

\[
Q_{Proposed} = \left\{2^{(N-M)} - 1\right\} + \left\{2^M(M-1) + 1\right\} \times 2^{(N-M)} I_{LSB}
\]

(10)

\[
= 575I_{LSB}
\]

So the Q value of the new architecture is less than segmented architecture, and hence the circuit shows better glitch energy performance.

### V. Random and Systematic Errors

The random error is determined solely by mismatch. The systematic errors are caused by process, temperature, and electrical gradients [6]. The systematic errors are layout-determined and are thus minimized during layout generation by optimizing the switching scheme and switching sequence. In layout the current blocks are placed in a 6 x 6 matrix for square shape. In optimally designed DACs, the INL and DNL are determined by random errors (i.e., mismatch) only. To see the effect of random variations on the static performance of the proposed and segmented architectures, simulation is done with MATLAB. Each of the current sources is given a random value that has been derived from a 2-D Gaussian distribution with a standard deviation of 0.02 LSB. The mean values of the unit current matrix A, B, C and D are \( I_{LSB}, I_{LSB}, 2I_{LSB} \) and \( 4I_{LSB} \) respectively. The dynamic behaviour of a DAC
mainly depends on the synchronization of the control signal of the switching transistors [6]. To see the effect of delay mismatch between the dynamic performance of the segmented and proposed architectures a MATLAB simulation is done. For a change in the input code the current switches going to turn OFF are delayed by a small time.

VI. PERFORMANCE ANALYSIS

Fig. 5 and Fig. 6 show the MATLAB simulated variations of DNL and INL respectively for proposed and segmented architectures.

![MATLAB simulated DNL of proposed and segmented DAC](image1)

Fig. 5. MATLAB simulated DNL of proposed and segmented DAC

![MATLAB simulated INL of proposed and segmented DAC](image2)

Fig. 6. MATLAB simulated INL of proposed and segmented DAC

The results are also checked with SPICE simulations and the proposed DAC shows improved DNL compared to its Segmented counterpart, whereas the INL of both DACs are comparable and the results are summarized in Table I. It can be seen from the Table I that the proposed architecture shows better dynamic performance than the segmented DAC. The dynamic performances for both architectures are MATLAB simulated for incoherent timing response. The current sources going to turn OFF are delayed by a small time to study the effect of delay mismatch on dynamic performances, and as a result of this, the simulated SNDR and SFDR are found to be relatively small. The proposed DAC shows better SNDR, THD and ERB [7] than the segmented DAC. The MATLAB simulated SFDR is same for both architectures.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>PERFORMANCES OF PROPOSED AND SEGMENTED DAC ARCHITECTURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Performance</td>
<td>Dynamic performances for sinusoidal input of frequency 10MHz sampled @ 500 MS/s</td>
</tr>
<tr>
<td>DNL</td>
<td>SNDR</td>
</tr>
<tr>
<td>Proposed Architecture</td>
<td>0.1373 LSB</td>
</tr>
<tr>
<td>Segmented Architecture</td>
<td>0.3015 LSB</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

In this paper, an 8-bit 1.8V 500 MS/s CMOS DAC for frequency domain applications is proposed. This DAC efficiently overcomes the main drawback of the segmented DAC, that is the delay mismatch between MSB block and LSB block control signal and IBT glitch. The proposed DAC shows improved DNL and better dynamic performance over segmented DAC. The prototype DAC is designed in 0.18μm double poly five-metal n-well CMOS process.

ACKNOWLEDGMENT

This work has been supported by ISRO and Ministry of Information Technology, Govt. of India. The authors would like to thank National Semiconductor for providing model files of 0.18μm CMOS technology.

REFERENCES