Low-power high-slew-rate CMOS buffer amplifier for flat panel display drivers

S.K. Kim, Y.-S. Son and G.H. Cho

A new high-slew-rate CMOS buffer amplifier consuming a very small quiescent current is proposed. This buffer amplifier recursively copies the output driving current and increases the tail current of the input differential pair during slewing. Since the proposed buffer has a possible slew rate higher than 10 V/μs for a load capacitance of 1 nF almost independently of static currents as low as 1 μA, this buffer amplifier is promising for column driver ICs of flat panel displays that require low static power consumption, high current driving capabilities, and small silicon areas.

Introduction: The columns of flat display panels using liquid crystal displays (LCDs) and organic light emitting diodes (OLEDs) are heavily capacitive electronically. Therefore, the active-matrix (AM) and passive-matrix (PM) LCDs, as well as voltage-driven AMOLEDs and PMOLEDs, require voltage buffer amplifiers in the column drivers. As the display resolution increases, the load capacitance of one buffer increases, whereas the required settling time decreases. In addition, hundreds of buffer amplifiers are integrated into one driver IC. Consequently, a high-slew-rate buffer amplifier with low static power consumption is indispensable. Although the class-AB folded-cascode operational amplifier described in [1] has been used widely as a buffer amplifier in the column driver, it only has a slew rate proportional to the input bias current. To increase the slew rate without wasting static current, several buffer amplifiers for the LCD column drivers have used additional class B- or C-type slew detectors [2–5]. In this Letter, we present a newly developed buffer amplifier that consumes a very low static current and has a high slew rate.

Proposed buffer amplifier

![Fig. 1 Proposed buffer amplifier](image)

Proposed circuit and operation: Fig. 1 shows the schematic of the proposed buffer amplifier. The circuit is composed of two parts. The upper part has an NMOS-input stage that drives the output PMOS MP for the sourcing current, and the lower part has a PMOS-input stage that drives the output NMOS MN for the sinking current. Each part has two positive-feedback loops and includes one negative-feedback loop. For the upper part, the positive-feedback loop 1 comprises M5–M10 and the positive-feedback loop 2 includes M1 and M11 merged into loop 1. Loop 1 influences the static state, whereas loop 2 is responsible for the high-slew-rate dynamic drive.

In the static state, since the input voltage and the output voltage are the same, the positive-feedback loop 2 of each part balances the negative-feedback loop comprising M9(A)-M11(A)-M2(A)-M8(A). Since the highest-impedance node of the total circuit is the output node, the load capacitance and resistance in the unity-gain negative-feedback loop perform the frequency compensation. On the other hand, $I_{AF(1)} = I_{AF(2)} + I_{AF(3)}$ and $I_{AF(4)} = I_{AF(4)}$ is in loop 1, therefore the current $I_{AF(1)}$ can be expressed as

$$I_{AF(1)} = I_{AF(2)} \times \left(\frac{1}{1 - k_2}\right)$$

(1)

where $k_1$ is the size ratio of M9(A) and M10(A), and it should satisfy $0 < k_1 < 1$. Then, the output current in the static state is calculated as

$$I_{out,static} = (0.5 \times I_{AF(1)} + k_2 \times I_{AF(2)}) \times k_3$$

(2)

where $k_2$ is the size ratio of M9(A) and M11(A), and $k_3$ is the size ratio of M5(A) and M10(A). The Early effect and mismatches of transistors are neglected, and $I_{AF2}$ and $I_{AF3}$ are assumed to be the same in this analysis. Note that by letting the constant current sources $I_{AF(1)}$ and $I_{AF(4)}$ be very small, e.g. tens of nanoamperes, the amplifier can be designed to consume a very low static current.

Fig. 2 Square-wave responses of buffer amplifier ($k_2 = 1$, $vbn2 = 1.0 V$, and $vbp2 = 2.2 V$)
a For a load capacitance of 1 nF
b For a load of modelled LCD column [7]

When there is a voltage difference in the differential input, a very high current can flow through either MP or MN, depending on the polarity of the input differential signal, by the operation of the positive-feedback loop 2. That is, loop 2 of the upper part operates when $V_{in} > V_{thn}$, whereas loop 2 of the lower part works when $V_{in} < V_{thn}$. The small currents $I_{AF(2)}$ and $I_{AF(4)}$ can be neglected in this dynamic state. For $k_2 \geq 1$, the output driving current increases until M5(A) and M6(A) enter the triode region, as long as a large differential input exists. For the case of $V_{in+} > V_{in-}$, the maximum sinking current is calculated as follows:

$$I_{M5A,max} = \frac{1}{2} k_2 \frac{W}{L} M5A \times (vbn2 - V_{thn} - V_{dsn})^2$$

(3)

$$I_{sinking,max} = k_3 \times I_{M5A} = k_3 \times \left(1 + \frac{k_2}{k_1}\right) \times I_{M7A,max}$$

(4)

where $V_{thn}$ is the drain–source voltage of M5A held in the triode region, and $V_{dsn}$ is the threshold voltage of NMOS. The Early effect and mismatches of transistors are neglected again. The parameters that control the maximum sourcing or sinking current are $vbp(n)2$, the size of M7(A), and the size ratios of $k_2$ and $k_3$. It should be noted that the preceding two
parameters can be designed independently of the static bias current, and the output current is still controlled even when $k_2 \geq 1$ [6].

Fig. 3 Variation of slew rate for load capacitance of 1 nF
- Falling slew rate for $k_2 = 2$
- Rising slew rate for $k_2 = 2$
- Falling slew rate for $k_2 = 1$
- Rising slew rate for $k_2 = 1$

Fig. 4 Performance comparison for load capacitance of 1 nF

Experiments and results: We manufactured the proposed buffer amplifier using a 0.35 μm CMOS process. The designed amplifier was biased to consume a current of 1 μA from the 3.3 V single supply. The steady-state errors between the input and output voltages were less than 10 mV in the entire operating region. Fig. 2 shows the slewing characteristics. Fig. 2a is for a load capacitance of only 1 nF, and Fig. 2b is for a load of an LCD panel model [7]. Fig. 3 verifies (3) and (4) by showing the variation of the slew rate according to the parameters $k_2$ and $v_{bn}(p)2$. Fig. 4 compares the performance of the designed buffer amplifier with those of other buffers for LCD drivers [2–5]. In this Figure, the comparison index was defined as the ratio of the slew rate to static power consumption. The performance of our buffer was measured under the conditions $k_2 = 1$, $vb2 = 1.0$ V, and $vb2p = 2.2$ V, while the slew rates reported in other work were converted for a load capacitance of 1 nF. Fig. 4 shows that the buffer amplifier designed in this work has a superior performance compared with other buffers, although it is not at its best. Furthermore, the buffer amplifier in this work requires a small silicon area owing to its simple configuration and the dispensability of additional compensation capacitors, and is thus more attractive for driver ICs of flat panel displays.

Conclusions: We have proposed, fabricated and measured a new high-slew-rate buffer amplifier that has great potential for applications in flat panel displays. The amplifier has a large current-driving capability by employing well-controlled positive current feedback loops and has control parameters for the maximum driving current.

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